PinE Training Academy

900+
PLACEMENTS

Summer Training in VLSI

Digital Design using Verilog & Implementation on FPGA

Give your core electronics dream a powerful boost.

PinE Training Academy

PinE Training Academy (Training Division of Aujus Technology Private Limited -Enabling VLSI Design) was established in 2014 by technocrats having expertise and vast work experience in the field of ASIC Design, FPGA, DSP, Real-Time Embedded System Design, and Board PCB.

For more info, visit - https://pinetrainingacademy.in/

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Meet Your Instructor

Vaibhav Mishra

(Founder at PinE Training Academy, Founder at Aujus Technology)

Vaibhav Mishra brings 21 years of experience in FPGA, semiconductor technologies, and engineering training.

He previously worked as a Field Application Engineer (FAE) for Xilinx FPGA, gaining strong experience in FPGA architecture, customer support, and application development.

His professional background includes:

- 10 years of experience as an FPGA FAE working closely with FPGA technology and ecosystem development
- 11 years of experience in mentoring and training engineers in VLSI, FPGA, and Embedded Systems
- Founder of Aujus Technology, an FPGA design house focused on hardware design and development services

Through his initiatives, Vaibhav has actively contributed to building a talent pipeline in FPGA, VLSI, and embedded technologies.

Summer Batch Certificate

Summer Batch Certification Test

Summer batch Industry Orientation

Summer Batch get-together

Summer Classes

Course Curriculum

Summer Training: VLSI

Module 1: - Hardware Digital Design - Hardware Design of various combinational & sequential circuits and implementation on FPGAs.

- **Project 1**: Hardware Design of 4-bit Sign Calculator and LED Implementation on FPGAs.
  - Calculator Components like: Adder, Subtractor, Multiplier, Divider, Comparator, Mux, Demux, Encoder, Decoder, 2s Complement, etc.
- **Project 2**: Hardware Design of a 4-way traffic light control system and SSD Implementation on FPGAs.
  - Traffic Light Components: Latch, SR Latch, JK latch, JK FF, DFF, TFF, counters (Synchronous, Asynchronous, UP- Down, Odd –Even, Mod, Johnson & Ripple, Shift Registers (SISO, SIPO, PISO & PIPO) & Frequency divider.
- **Project 3**: Hardware Design of different LED Patterns & LED Implementation on FPGAs.
- **Project 4**: Hardware Design of Digital Clock & SSD Implementation on FPGAs.
- **Project 5**: Hardware Design of Stop watch & SSD Implementation on FPGAs.
- **Project 6**: Schematics Design of Algebra and Geometry Formulas
- Introduction to FPGA & CPLD & Application of FPGA & CPLD
- Development Board: Nexys A7, Artix 7 series development board from Digilent Inc.

Course Curriculum

Summer Training: VLSI

Module 2: - Verilog and implementation on FPGAs.

- Introduction of RTL & FPGA Flow & Introduction of Verilog.
- Methodologies
  - Gate Level
  - Data Flow
  - Behavioural: Blocking & Non - Blocking & IF Else & Case
  - Synthesis - RTL Flow,, Technology Flow
  - Test bench
- Programming: Implementation of all combinations and sequential circuits on an FPGA using Verilog.
- **Project 1** : FIFO & LIFO designing using Verilog and LED & SSD Implementation on FPGA's.
- **Project 2**: LED Blinker design using Verilog and LED Implementation on FPGAs.
  - The Internship Project will be awarded by Aujus Technology, depending on the performance and ability to finish the project in time.

Program objective of Internship Course Name: Verilog Programming & FPGA Internship Course (1 Month) Program in VLSI:

- Understanding Digital Design, Verilog & FPGA Design
- Hands-on Experience Design & Optimisation Techniques
- Industry-Relevant Skills & Project Development
- Networking and Industry Exposure

Summary of the program:

- **Introduction to VLSI Flow**: Through this training, trainees will be able to identify their areas of interest within VLSI.
- Once they have identified their areas of interest, trainees can develop expertise in those areas within one year.
- After gaining expertise, trainees will be prepared to seek placements in their chosen domains.
- 100% hands-on session from the first day of the training
- Focus on Major and minor project-based internships
- From this training, students can identify their final-year project
- The tools and Hardware board will be provided by the academy only

Key takeaways from the summer training program:

- How to develop a logical approach using digital components in hardware design and the implementation of an FPGA?
- Hardware Circuit design using digital components of Real-time applications like a signed calculator, multiplier, divider, digital clock, stopwatch timer and LED blinker.
- Understanding of FPGA Architecture from Idea to Programming in both hardware design using Verilog
- Understanding and basic knowledge of functional and Behavioural, simulation, synthesis and implementation.

Course Information:

- **Who Can Join**: Pursuing 1st (optional) 2nd Year B. Tech and M. Tech 1st Year
- B**ranch**: Electronics & Electricals Engineering
- **Mode**: Offline and Online || Batch Size: 20 Trainees
- **Course starts every year**: 15th May / 15th June
- **Duration**: 45 days
- The Institute has the full right to select the modules as per the requirements of the industry, and also depends on the duration of the batch, without affecting the course fees.
- Certification test is mandatory to attend to receive the certificate.
- Internship project & certificate will be offered only to the performers or those who have completed the industry project.

Course Fees

- Hardware Digital Design & Implementation on FPGA – Rs 2950
- HDL – Verilog & Implementation on FPGA Level -1- Rs 2950
- Certification – No Cost
- Project-based internship and certificate – No Cost

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