Foundation Course VLSI Level -1

Course Module

- Course Name: **Skill Foundation in VLSI** Level -1
- Who Can Join: Pursuing 2nd Year B. Tech and M. Tech & M. Sc -1st Year
- **The Institute has full right to select the modules as per the requirement of the industry and also depend on the duration of the batch without affecting the course fees.**
- **Certification test is mandatory to attend to award the certificate.**
- **Internship will offer only to the performers or those who completed the industry project.**
- **Fees of each module is**
  - **Hardware Digital Design @ Rs 2950**
  - **HDL – Verilog @Rs 2950**
  - **RC & Network @Rs 2950**
  - **C & C++ Programming @2950**

Total Fees for Level 1@ Rs 11800

1. **Module 1- Hardware Digital Design - Hardware Design of various combinational & sequential Circuit and implementation on FPGA's.**
   - Project 1: Hardware Design of 4-bit Sign Calculator and LED Implementation on FPGA's.
     - ✓ Calculator Components like: Adder, Subtractor, Multiplier, Divider, Comparator, Mux, Demux, Encoder, Decoder, 2s Complement etc.
   - Project 2: Hardware Design of 4-way traffic light control system and SSD Implementation on FPGA's.
     - ✓ Traffic Light Components: Latch, SR Latch, JK latch, JK FF, DFF, TFF, counters (Synchronous, Asynchronous, UP- Down, Odd –Even, Mod, Johnson & Ripple, Shift Registers (SISO, SIPO, PISO & PIPO) & Frequency divider.
   - Project 3: Hardware Design of different Led Pattern & LED Implementation on FPGA's.
   - Project 4: Hardware Design of Digital Clock & SSD Implementation on FPGA's.
   - Project 5: Hardware Design of Stop watch & SSD Implementation on FPGA's.
   - Project 6: Schematics Design of Algebra and Geometry Formulas
   - Introduction to FPGA & CPLD & Application of FPGA & CPLD
   - Development Board: Nexys A7, Artix 7 series development board from Digilent inc.

2. **Module 2- Verilog**
   - Introduction of RTL & FPGA Flow & Introduction of Verilog.
   - Methodologies
     - ✓ Gate Level
     - ✓ Data Flow
     - ✓ Behavioural
       - ➢ Blocking & Non-Blocking & IF Else & Case
     - ✓ Synthesis
       - ➢ RTL Flow
       - ➢ Technology Flow
   - Programming : Implementation of all combination & sequential circuit on FPGA using Verilog.
   - Project 1 : FIFO & LIFO designing using Verilog and LED & SSD Implementation on FPGA's.

- Project 2 : LED Blinker designing using Verilog and LED Implementation on FPGA's.

➢ **The Internship Project will be awarded from Aujus Technology, depending on the performance and ability to finish the project in time.**

3. **Module 3**- RC & Network -Introduction of network elements and its properties.
   - Understanding the fundamental of KCL, KVL, Source Transformation, Resistance equivalent, Star to Delta and Delta to star transformation, and it's numerical.
   - Understanding of Theorems like Thevenin, Norton, Super-position and Maximum Transfer Theorem and it's numerical.
   - Understanding of RC circuit with different sources.
   - Introduction of Electronic Device circuit.
4. **Module 4** – C & C ++ Programming Implementation of LIFO memory (STACK (software))

   C Programming
   - **Introduction -**
     - ✓ "Hello World" Program - Getting Started
     - ✓ Working with Code Blocks
     - ✓ Variables and Arithmetic Expressions
     - ✓ Character Input and Output
     - ✓ File Copying
     - ✓ Examples with Character Counting, Line Counting, Word Counting

   C ++ Programming
   - Introduction to Class-
     - ✓ "Hello World Program"
     - ✓ Types, Variables, and Arithmetic
     - ✓ Constants
     - ✓ Tests and Loops
     - ✓ Pointers, Arrays, and Loops
     - ✓ Public and Private Elements
     - ✓ Structure, Classes
     - ✓ Modularity

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