PinE Training Academy

900+
PLACEMENTS

VLSI

Design For Testability

Offline | Hybrid | Online

Academic qualification for this course:

B.Tech /M.Tech with min 70 % through out in ECE /EEE/VLSI

Cadence Tool Lab Support

Placement Assistance

1:1 Mentoring

PinE Training Academy

PinE Training Academy (Training Division of Aujus Technology Private Limited -Enabling VLSI Design) was established in 2014 by technocrats having expertise and vast work experience in the field of ASIC Design, FPGA, DSP, Real-Time Embedded System Design, and Board PCB.
For more info, visit - https://pinetrainingacademy.in/

Hiring Partners

SYNOPSYS® · SignOff semiconductors · cadence® · KEENHEADS · CIRCUIT SUTRA TECHNOLOGIES · Vervesemi · AUJUS TECHNOLOGY · SIEMENS

"At PinE Training Academy, my vision has always been to help electronics students move beyond theoretical learning and **develop the practical skills** required by the industry.

Having worked closely with students and companies for years, **I have seen the gap between academic education and real engineering roles.**

PinE was built to bridge that gap — by providing structured learning, strong fundamentals, and guided career pathways so that **students can confidently step into core engineering careers.**"

- Vaibhav Mishra
(Founder & CEO)

To know more about our CEO, visit https://www.linkedin.com/in/vaibhav-mishra-1b01951/

Top 5 reasons to choose PinE Training Academy

1. 100% Placement Support

PinE provides 100% placement assistance to the eligible trainees of the job-oriented programs and keeps supporting them till they get a job after course completion. Our primary objective is to help electronics engineers successfully build a career in the semiconductor /VLSI Industries. We work closely with various VLSI products & services companies and identify the right opportunities. Most of our students have been successfully placed in reknowned semiconductor companies.

2. VLSI courses delivered by industry experts

PinE Training Academy is a leading VLSI and Embedded training institute that delivers industry-standard, high-quality VLSI programs. Our courses are designed by experienced industry experts, aligned with real job opportunities and long-term career growth in the semiconductor sector. We continuously update our VLSI curriculum to match the latest industry trends.

3. Excellent Teaching Methodology

Our training methodology is unique, enabling students to master even complex technologies in a short time and build true expertise. Around 70% of the course is dedicated to hands-on labs, mini projects, and a final project. These programs help you develop the in-demand technical skills needed to secure a job in the semiconductor industry.

4. 1:1 Support

PinE Training Academy provides 1:1 mentoring and round-the-clock online support Trainees also get 24/7 lab access to strengthen their technical skills and can join group discussions to learn and share insights. In addition, business communication sessions and mock interviews help build the professional skills needed to succeed in the workplace.

5. Flexible Payment & Financial Support

- Merit-Based Scholarship Program
- Interest-Free Monthly Installments
- Education Loan from NBFC Partners
- Auto-Debit Facility

EDA Partner

cadence

Get trained on Cadence industry grade tools and showcase your knowledge confidently in your interviews.

COURSE CURRICULUM

Design For Testability (DFT)

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21 modules

OS- Linux Ubuntu | EDA Tool - Cadence

1. Hardware Digital Design

- Hardware Design of various combinational & sequential circuits and implementation on FPGAs.
- Project 1: Hardware Design of 4 bit Sign Calculator and implementation on FPGAs.Calculator Components like: Adder, Subtractor, Multiplier, Divider, Comparator, Mux, Demux, Encoder, Decoder,2s Complement etc.
- Project 2: Hardware Design of 4 way traffic light control system and implementation on FPGAs.
- Traffic Light Components: Latch, SR Latch, JK latch, JK FF, DFF, TFF, Counters (Synchronous , Asynchronous , UPDown Odd –Even , Mod , Johnson & Ripple, Shift Registers (SISO, SIPO , PISO & PIPO)
- Project 3: Hardware Design of different Led Patterns & Implementation on FPGAs.
- Project 4: Hardware Design of FIFO & LIFO Implementation on FPGAs.
- Project 5: Hardware Design of Digital Clock and Stopwatch & Implementation on FPGAs.

2. CPLD & FPGA Introduction

- Introduction to FPGA & CPLD
- Application of FPGA & CPLD
- Advantage & Disadvantage of FPGA & CPLD
- CPLD & FPGA Architecture
- FPGA & FLOW
- Development Board: Nexys A7, Artix 7 series development board from Digilent inc.

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3. Analog Network

- Fundamentals of Network
  - -Condition of flow of current
  - -Power consumption and Telegans theorem
  - -Resistance
  - -Electrical Energy Sources
  - -node, mesh and loops
  - -Kirchoff law
  - -Voltage division principle
  - -currrent division principle
  - -source transformation
  - -resistance reduction techniques
  - -mesh analysis
  - -nodal analysis
- Network Theorems
  - -Linear theorem
  - -Thevenin
  - -Norton
  - -max power theorem
- Inductor
- Capacitor
- DC Transient Analysis

4. Analog EDC (Electronics Design Circuits)

- Drift current
- Diffusion current

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- Channel width and effect on it by various factor
- P-N junction
- Diode fundamentals
- MOSFET operation
- Leakage current
- Effects on operation by doping and temp
- Temp inversion

5. Verilog

- Introduction of RTL & FPGA Flow.
- Introduction of Verilog.
- Methodologies
  - -Gate Level
  - -Data Flow
  - -Behavioral
  - -Test Bench
  - -FSM Modeling
  - -Synthesis- RTL Flow, Technology Flow
- Programming : Implementation of all combinational & sequential circuits on FPGA using Verilog.
- Project 1 : LED Implementation of 4bit Sign calculator on FPGA using Gate level Verilog.
- Project2 : SSD Implementation of Traffic Light Controller on FPGA using Behavioral FSM Modeling
- Project 3 : SSD Implementation of Digital Clock on FPGA using Verilog.
- Project 4 : SSD Implementation of Stop watch on FPGA using Verilog

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6. UNIX

- The Basics of UNIX and how it's different from Windows.
- Introduction of SHELL.
- File and Directories.
- Home Directory and .xshrc files (.bashrc, .cshrc, etc.)
- Introduction to inode
- Types of files, symbolic and hard links
- Permissions of files, timestamps in unix.
- Basic Commands-cp, mv, rm, touch, which, mkdir ,cat, find, cut, paste, tr, ls, ps, sort, etc.
- Sed, awk, grep (regex), commands.

7. BASH

- Shell scripting, structure of a script, usage of loops, conditional statements, functions, arguments and array.

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8. TCL-TK

- TCL:
  -Set ,Puts
  -String cmd & its various options compare ,equal, first, last ,index, is class, length, map, match, range, repeat, replace, reverse, tolower, toupper, totitle, trim, trimleft, trimright, wordstart, wordend.
  -List and its various options lappend, lindex, linsert, llength, lmap, lrange, lrepeat, lreplace, lreverse, lsearch, lset, lsort, Concat, Format, Scan, Glob, Global, Incr, Expr, Join, Split, foreach loop, If loop, for loop, switch, while loop, catch, clock, regexp, regsub
  -Tcl procedures- return,non return, args,optional arguments etc.
  -file handling:- open & close
  -file command and its various options, argc,argv,argv0, arrays, upvar, after, Namespaces Source, Unset, Exec, Exit, Flush, Time, Break, Continue, Read
- TK:
  -Basics of TK (Tool Kit), wish interpreter, advantages of T
  -Widgets, types of widgets (basic, hierarchical), selection widget, frame widget, pack proapgate, text widget, scrollbar widget, canvas widget, bitmaps, fonts, tk_messageBox.

9. VLSI Design Flow (RTL-GDS) [Basic Overview]

- RTL Logic Synthesis
- Netlist
- Physical Design GDS

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10. Verification and Testing [Basic Overview]

- Fault Models
- Scan Insertion
- Built-In Self-Test (BIST)
- Automatic Test Pattern Generation (ATPG)
- Boundary Scan Testing
- Test Compression
- Test Compression Techniques
- Fault Coverage
- Design Rules
- Verification Process

11. Importance of Testing

- Overview
- Defects
- Terminologies

12. Design for Test

- Terminologies
- Fault Models

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13. Test Vectors

- Scan Design Flow
- Controllability & Observability
- Scan cells & Scan Chain

14. Working and Testing Modes

- Functional mode vs test mode
- Scan enable / test control signals
- Scan flip-flop operation
- Shift and capture phases
- Controllability and observability
- Test application flow
- Clock behavior in test mode
- Mode-specific design concerns

15. ATPG

- Objectives & Challenges
- Approach & Working

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16. BIST

- Introduction to BIST
- Types of BIST
- Basic BIST architecture
- Pattern generation methods
- Response checking
- Logic BIST topics
- Memory BIST topics
- BIST control and modes
- Advantages and limitations of BIST

17. Industrial Flow

- DFT Tools
- Design Steps
- Industrial example

18. Fault Injection

- New Domain
- Questions for DFT

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19. Perl

- Perl basic concepts and Syntax
- Different Data Types and Data Structure of Perl
- Regex
- File Handling and Error Handling
- Perl Packages
- Scoping of variable
- Subroutines

20. Python

- Basic concepts
- Python Data types
- Python Loop
- Python Function
- Python Lambda
- Python Regex
- Python OOPS

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21. STA Fundamentals

- What is STA and why we need to do STA in the flow
- Inputs and outputs of STA.
- Different types of STA terminologies
- What are Setup and Hold time and its Mathematical equations.
- Setup and hold time calculation with examples
- Different techniques used to fix setup and hold issue in the different stages.

Note- The Institute has full right to select the modules as per the requirement of the industry and also depend on the duration of the batch without affecting the course fees

Course Information

New batch starts every

January | April | July | October

Course Duration

- Offline - **6 months**
- Hybrid - **10 months**
- Online - **12 months**

Course Fees

The fees will vary for different modes-online, hybrid and offline and can range between INR 90k - 1.15lacs + tax

Scholarship

The scholarship will be given based on the entrance test.

Score 90% or above - **40% scholarship**
Score 75% or above - **20% scholarship**

Prerequisite for Entrance Test: Basic Knowledge of Analog & Digital Design Fundamentals

PinE Training Academy

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