PinE Training Academy

900+
PLACEMENTS

FPGA

Offline | Hybrid | Online

Academic qualification for this course:

B.Tech /M.Tech with min 70 % through out in ECE /EEE/VLSI

Cadence Tool Lab Support

Placement Assistance

1:1 Mentoring

PinE Training Academy

PinE Training Academy (Training Division of Aujus Technology Private Limited -Enabling VLSI Design) was established in 2014 by technocrats having expertise and vast work experience in the field of ASIC Design, FPGA, DSP, Real-Time Embedded System Design, and Board PCB.
For more info, visit - https://pinetrainingacademy.in/

Hiring Partners

SYNOPSYS · SignOff semiconductors · cadence · KEENHEADS · CIRCUIT SUTRA TECHNOLOGIES · Vervesemi · AUJUS TECHNOLOGY · SIEMENS

"At PinE Training Academy, my vision has always been to help electronics students move beyond theoretical learning and **develop the practical skills** required by the industry.

Having worked closely with students and companies for years, **I have seen the gap between academic education and real engineering roles.**

PinE was built to bridge that gap — by providing structured learning, strong fundamentals, and guided career pathways so that **students can confidently step into core engineering careers.**"

- Vaibhav Mishra
(Founder & CEO)

To know more about our CEO, visit https://www.linkedin.com/in/vaibhav-mishra-1b01951/

Top 5 reasons to choose PinE Training Academy

1. 100% Placement Support

PinE provides 100% placement assistance to the eligible trainees of the job-oriented programs and keeps supporting them till they get a job after course completion. Our primary objective is to help electronics engineers successfully build a career in the semiconductor /VLSI Industries. We work closely with various VLSI products & services companies and identify the right opportunities. Most of our students have been successfully placed in reknowned semiconductor companies.

2. VLSI courses delivered by industry experts

PinE Training Academy is a leading VLSI and Embedded training institute that delivers industry-standard, high-quality VLSI programs. Our courses are designed by experienced industry experts, aligned with real job opportunities and long-term career growth in the semiconductor sector. We continuously update our VLSI curriculum to match the latest industry trends.

3. Excellent Teaching Methodology

Our training methodology is unique, enabling students to master even complex technologies in a short time and build true expertise. Around 70% of the course is dedicated to hands-on labs, mini projects, and a final project. These programs help you develop the in-demand technical skills needed to secure a job in the semiconductor industry.

4. 1:1 Support

PinE Training Academy provides 1:1 mentoring and round-the-clock online support Trainees also get 24/7 lab access to strengthen their technical skills and can join group discussions to learn and share insights. In addition, business communication sessions and mock interviews help build the professional skills needed to succeed in the workplace.

5. Flexible Payment & Financial Support

- Merit-Based Scholarship Program
- Interest-Free Monthly Installments
- Education Loan from NBFC Partners
- Auto-Debit Facility

EDA Partner

cadence

Get trained on Cadence industry grade tools and showcase your knowledge confidently in your interviews.

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OS- Linux Ubuntu | EDA Tool - Cadence

1. Hardware Digital Design

- Hardware Design of various combinational & sequential circuits and implementation on FPGAs.
- Project 1: Hardware Design of 4 bit Sign Calculator and implementation on FPGAs.Calculator Components like: Adder, Subtractor, Multiplier, Divider, Comparator, Mux, Demux, Encoder, Decoder,2s Complement etc.
- Project 2: Hardware Design of 4 way traffic light control system and implementation on FPGAs.
- Traffic Light Components: Latch, SR Latch, JK latch, JK FF, DFF, TFF, Counters (Synchronous , Asynchronous , UPDown Odd –Even , Mod , Johnson & Ripple, Shift Registers (SISO, SIPO , PISO & PIPO)
- Project 3: Hardware Design of different Led Patterns & Implementation on FPGAs.
- Project 4: Hardware Design of FIFO & LIFO Implementation on FPGAs.
- Project 5: Hardware Design of Digital Clock and Stopwatch & Implementation on FPGAs.

2. CPLD & FPGA Introduction

- Introduction to FPGA & CPLD
- Application of FPGA & CPLD
- Advantage & Disadvantage of FPGA & CPLD
- CPLD & FPGA Architecture
- FPGA & FLOW
- Development Board: Nexys A7, Artix 7 series development board from Digilent inc.

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3. UNIX

- The Basics of UNIX and how it's different from Windows.
- Introduction of SHELL.
- File and Directories.
- Home Directory and .xshrc files (.bashrc, .cshrc, etc.)
- Introduction to inode
- Types of files, symbolic and hard links
- Permissions of files, timestamps in unix.
- Basic Commands-cp, mv, rm, touch, which, mkdir ,cat, find, cut, paste, tr, ls, ps, sort, etc.
- Sed, awk, grep (regex), commands.

4. TCL-TK

- TCL:
  -Set ,Puts
  -String cmd & its various options compare ,equal, first, last ,index, is class, length, map, match, range, repeat, replace, reverse, tolower, toupper, totitle, trim, trimleft, trimright, wordstart, wordend.
  -List and its various options lappend, lindex, linsert, llength, lmap, lrange, lrepeat, lreplace, lreverse, lsearch, lset, lsort, Concat, Format, Scan, Glob, Global, Incr, Expr, Join, Split, foreach loop, If loop, for loop, switch, while loop, catch, clock, regexp, regsub
  -Tcl procedures- return,non return, args,optional arguments etc.
  -file handling:- open & close
  -file command and its various options, argc,argv,argv0, arrays, upvar, after, Namespaces Source, Unset, Exec, Exit, Flush, Time, Break, Continue, Read
- TK:
  -Basics of TK (Tool Kit), wish interpreter, advantages of T
  -Widgets, types of widgets (basic, hierarchical), selection widget, frame widget, pack proapgate, text widget, scrollbar widget, canvas widget, bitmaps, fonts, tk_messageBox.

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5. BASH

- Shell scripting, structure of a script, usage of loops, conditional statements, functions, arguments and array.

6. Verilog

- Introduction of RTL & FPGA Flow.
- Introduction of Verilog.
- Methodologies
  - -Gate Level
  - -Data Flow
  - -Behavioral
  - -Test Bench
  - -FSM Modeling
  - -Synthesis- RTL Flow, Technology Flow
- Programming : Implementation of all combinational & sequential circuits on FPGA using Verilog.
- Project 1 : LED Implementation of 4bit Sign calculator on FPGA using Gate level Verilog.
- Project2 : SSD Implementation of Traffic Light Controller on FPGA using Behavioral FSM Modeling
- Project 3 : SSD Implementation of Digital Clock on FPGA using Verilog.
- Project 4 : SSD Implementation of Stop watch on FPGA using Verilog

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7. VHDL

- Introduction of RTL Flow
- Introduction of VHDL
- Methodologies
  - Structural Modeling
  - Data Flow Modeling
  - Behavioural Modeling
  - Mixed Modeling
  - Test bench
  - FSM Modeling
  - Synthesis: RTL Flow, Technology Flow
- Enumerated Types
- Packages
- Sub Programs
- Function & Procedure
- Programming : Implementation of all combination & sequential circuit on FPGA using Verilog.
- Project 1 : LED Implementation of 4bit Sign calculator on FPGA using Gate level Verilog.
- Project2 : SSD Implementation of Traffic Light Controller on FPGA using Behavioural FSM Modeling
- Project 3 : SSD Implementation of Digital Clock on FPGA using Verilog.
- Project 4 : SSD Implementation of Stop watch on FPGA using Verilog
- Project 5 : Interface based Project:
- Project 6 : VGA Interface
- Project 7 : UART Interface
- Project 8 : Key board Interface
- Project 9 : LCD Interface
- Project 10 : Temperature Sensor using Xilinx xADC

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8. Introduction of FPGA Architecture

- FPGA: - Xilinx Spartan 6/Virtex 6 Basic FPGA Architecture.
  - CLB architecture.
  - LUT architecture.
  - Slices.
  - Wide Multiplexer.
  - I/O Bank Structure.
  - Clock Managers.
  - CMT/PLL (Virtex 6).
  - Block RAM Memories.
  - External Memory Controller Block (Spartan 6).
  - Configuration.
  - DSP Slices.
  - High Speed Transceivers.
  - PCI Express.
  - TEMAC
  - System Monitor.
- Exposure of Xilinx Development Board:-Spartan 6 SP601/SP605/ Artix – Nexys 7 / Basys 3 Interface :-
  - UART.
  - JTAG.
  - FLASH SPI/BPI.
  - DIP Switch.
  - Configuration Mode.
  - LED.
  - LCD.
  - Seven Segment.
  - USB.
  - FMC.
  - Ethernet.
  - PCI.
  - SMA.
  - SFP.

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9. FPGA Design Flow – ISE/Vivado

- Design technique.
  - Simulation.
  - ISIM.
- Synthesis.
  - Pre- Synthesis Simulation.
  - Post Synthesis Simulation.
  - Synthesis Technique.
  - Analysis of Report.
- Planahead.
  - UCF- I/O Planning.
  - Timing Constraint.
- Implementation.
  - Translation: Post Translation Simulation.
- Mapping.
  - Post Mapping Simulation.
- Placement and Routing.
  - Post Placement and Routing Simulation.
- Implementation Technique and Analysis of Report at each stage.
- Programing.
  - FPGA Programming.
  - FLASH Programming.

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10. Tools Technique ISE/Vivado

- Understanding and Practical Exposure on Tools:-
  - Coregen/IP catalogue.
  - ChipScope all type
- Planahead.
  - Area Planning.
  - Floor Planning.
  - I/O Planning.
- Design Goal and Strategies.
- Smart Guide.
- Timing Analysis.
  - SDC Constraint using Vivado.
- Power Analyzer.
- Smart Xplorer.
- iMPACT.

11. FPGA Embedded Architecture

- Embedded System.
  - Introduction to Embedded System.
  - Component of Embedded System.
  - Embedded Processor.
- Embedded Support on FPGA
  - Hard/Soft IPs.
  - Dedicated hard IPs on FPGA.
  - BRAM, PCI, Ethernet

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- ZYNQ Architecture.
  - Introduction to ZYNQ.
  - Programmable Logic.
  - Programmable System.
  - ARM Cortex A9 architecture.
  - PS-PL Inter-connection.
- Xilinx Tools for Embedded Design.
  - Embedded Design Flow.
  - EDK/SDK tool flow.
  - EDK project creation.
  - IP Catalogue.
  - Custom IP integration.
- Xilinx C libraries for FPGA.
  - Data types.
  - Function.
  - Controls
  - Loops
  - Structure & file handling.
- Example/exercise on EDK tools flow.

12. Embedded System on ZYNQ

- Project Creation in EDK/SDK.
- Custom IP and integration lab
- Device Drivers.
- Example/Exercise on ZYNQ – ZED Board and AVNET ZYNQ Development board Z7010.

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13. Embedded C

- C programing Steps.
  - Introduction to cross compilation.
  - Assembler.
  - Memory segmentation.
  - Linkers & executable.
- Elements of C programing (review).
  - Data types.
  - Function.
  - Controls.
  - Loops.
  - Structure.
  - File handling.
- Xilinx C libraries for FPGA.
  - Data types.
  - Function.
  - Controls
  - Loops
  - Structure & file handling.

14. Embedded Linux

- Introduction to Embedded Linux.
  - Embedded Linux system architecture
  - Linux Kernel Architecture.
  - Memory Organization.
  - File system.
  - Linux Start Sequence.
  - BSPs.

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- Embedded Linux Porting Concepts.
  - Cross-Compilation & GNU cross tool chains.
  - Porting Road map.
  - U-boot.
  - Various format of kernel Image.
- Embedded Linux on ZYNQ.
  - Storage support on ZYNQ.
  - Booting option for ZYNQ.
  - Exercise on porting Linux on ZYNQ.

15. Introduction to DSP Tools and Data Types

- Introduction of Matlab and Simulink.
- FPGAs for DSP.
- Introduction to System Generator.
- Simulink Basics.
- Arithmetic Operations.
- Fixed Point Format-Signed and Unsigned (with or without binary point).
- Gateway In & Out.
- Saturation and Wrap in fixed point numbers.
- Applications of Round and Truncate in fixed point while arithmetic operations.
- Hardware Cost of Saturation, Wrap, Round and Truncation.
- Addition, Subtraction, Multiplication, Division, Scaling and Shifting.
- Complex arithmetic- Complex multiplication, conjugate etc.

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16. Block sets Library

- Library Overview
- Use of blocks available inside Xilinx Block sets' Library- Basic blocks.
- Handshaking blocks- FIFO, BLOCK RAM etc.
- Signal Processing Blocks- FFT, FIR etc.
- Data storing blocks- ROM.
- Black Box- HDL import.
- CORDIC
- Arithmetic Functions in Circular Co-ordinates.
- Implementations.
- CORDIC Complier.
- Test and Interview Series.

17. Signal Generation within FPGA

- NUMERICALLY CONTROLLED OSCILLATOR (NCO).
- Look Up Table Technique.
- DDS Compiler and Phase Truncation techniques.
- Sine wave generation using DDS Compiler.
- Applications.

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18. Single Rate & Multi-Rate Filtering

- FIR & IIR Filtering
- Sampling, Sub-Sampling, Nyquist-Criterion, Mixing, Quadrature Modulator &I-Q.
- Single Rate and Multi-Rate Filters, MAC filters.
- Interpolation and Decimation.
- Difference between Up sampling, Interpolation, Down sampling and Decimation.
- Half- Band Filters and its implementation.
- Interpolation FIR filter and its implementation using FDA Tool.
- Decimation FIR Filter- with various windowing techniques and its implementation using FDA Tool.
- Poly-Phase Filters.
- IIR Filter and its implementation using FDA Tool.
- Effects of Quantization and importance of ENOB.
- LOW PASS CASCADED INTEGRATED COMB (CIC) FILTERS.
- Brief Overview of Decimation and Interpolation.
- CIC Filters Theory and its Construction.
- Interpolation and Decimation with CIC.
- CIC Compiler.
- Compensation FIR Filter.
- Test and Interview Series.

19. DIGITAL UPCONVERSION & DOWNCONVERSION

- DUC & DDC DESIGN IN SYSTEM GENERATOR.
- Digital Up Convertors and Digital Down Convertors.
- Implementation Using either FIR filters or CIC filters,
- SNR improvement in DDC.

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20. MODEM DESIGN USING DSP

- INTRODUCTION TO ANALOG AND DIGITAL COMMUNICATION.
- Analog modulation schemes.
- Analog Transmitter- AM-SSB/AM-DSB/FM.
- Analog Receiver- AM-SSB/AM-DSB/FM.
- Basic Modulation Schemes like PSK, FSK, QAM, OFDM etc.
- PSK based Modulator.
- Pulse Shaping and Matched Filtering and its implementation.
- PSK based Demodulator.
- Communication Link.
- Channels and Channel Equalization.
- Eb/No Vs BER plots for PSK schemes.

21. HARDWARE CO-SIM

- HARDWARE CO-SIM & USE OF CHIPSCOPE ANALYZER.
- Analyze Design using Timing and Power Report.
- Creating HDL.
- Creating NGC.
- Creating Bit stream.
- Analyze Complete Design using CHIPSCOPE ANALYZER.
- Hardware Co-Simulations.
- Test and Interview Series.

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22. Perl

- Perl basic concepts and Syntax
- Different Data Types and Data Structure of Perl
- Regex
- File Handling and Error Handling
- Perl Packages
- Scoping of variable
- Subroutines

23. Python

- Basic concepts
- Python Data types
- Python Loop
- Python Function
- Python Lambda
- Python Regex
- Python OOPS

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24. Network

- Fundamentals of Network
  - -Condition of flow of current
  - -Power consumption and Telegans theorem
  - -Resistance
  - -Electrical Energy Sources
  - -node, mesh and loops
  - -Kirchoff law
  - -Voltage division principle
  - -currrent division principle
  - -source transformation
  - -resistance reduction techniques
  - -mesh analysis
  - -nodal analysis
- Network Theorems
  - -Linear theorem
  - -Thevenin
  - -Norton
  - -max power theorem
- Inductor
- Capacitor
- DC Transient Analysis

25. Analog EDC (Electronics Design Circuits)

- Drift current
- Diffusion current

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- Channel width and effect on it by various factor
- P-N junction
- Diode fundamentals
- MOSFET operation
- Leakage current
- Effects on operation by doping and temp
- Temp inversion

26. STA Fundamentals

- What is STA and why we need to do STA in the flow
- Inputs and outputs of STA.
- Different types of STA terminologies
- What are Setup and Hold time and its Mathematical equations.
- Setup and hold time calculation with examples
- Different techniques used to fix setup and hold issue in the different stages.

Note- The Institute has full right to select the modules as per the requirement of the industry and also depend on the duration of the batch without affecting the course fees

Course Information

New batch starts every

January | April | July | October

Course Duration

- Offline - **6 months**
- Hybrid - **10 months**
- Online - **12 months**

Course Fees

The fees will vary for different modes-online, hybrid and offline and can range between INR 50k - 75k + tax

Scholarship

The scholarship will be given based on the entrance test.

Score 90% or above - **40% scholarship**
Score 75% or above - **20% scholarship**

Prerequisite for Entrance Test: Basic Knowledge of Analog & Digital Design Fundamentals

PinE Training Academy

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